



2184

Parson 3-2-1-4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): D.E. Parson et al.
Case: 3-2-1-4
Serial No.: 09/583,057
Filing Date: May 30, 2000
Group: 2184
Examiner: Timothy M. Bonura

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature: James M. Hanley Date: June 13, 2003

Title: Control Method and Apparatus for Testing of Multiple Processor Integrated Circuits and Other Digital Systems

TRANSMITTAL LETTER

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith is the following document relating to the above-identified patent application:

(1) Response to Office Action.

There is no additional fee due in conjunction with the response. In the event of any non-payment or improper payment of a required fee, the Commissioner is hereby authorized to charge or to credit **Ryan, Mason & Lewis, LLP Deposit Account No. 50-0762** as required to correct the error.

Respectfully submitted,

Date: June 13, 2003

Joseph B. Ryan
Attorney for Applicant(s)
Reg. No. 37,922
Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560
(516) 759-7517

RECEIVED
JUN 20 2003
TECHNOLOGY CENTER 2800